UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 09/991,341 | 11/16/2001 | Chang Cheng Hung | 67,200-435 | 3529 |

7590 07/01/2005

TUNG & ASSOCIATES
Suite 120
838 W. Long Lake Road
Bloomfield Hills, MI 48302

| EXAMINER | |
|---|---|
| CHAWAN, SHEELA C | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2625 | |

DATE MAILED: 07/01/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. 09/991,341 | Applicant(s) HUNG ET AL. | |
|---|---|---|---|
| | Examiner Sheela C. Chawan | Art Unit 2625 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *04 February 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-7 and 10-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7 and 10-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Response to Amendment*

1. Applicant's amendment filed on Feb 4, 2005 has been entered and made of record.

Claims 8- 9 and 20 are canceled claims.

Claims 1-7, 10-19, are pending in the application.

### *Response to Arguments*

2. Applicant's arguments, see page 7 lines 11- 13, filed Feb 4, 2005, with respect to rejection of claims 1-20 under 102(e) have been fully considered and are persuasive. The 102(e) rejection of claims 1-20 has been withdrawn.

Applicant's arguments see pages 11-13 of the remarks, filed 11/12/04, with respect to the rejection of claims 1-20 under 102 (e) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of MacDonald, Jr. et al., and (US 4,131, 472).

### *Claim Objections*

3. Claim 11 is objected to because of the following informalities:

In claim 11, line 1, change " 9 " to -- 1 -- .

Appropriate correction is required.

***Claim Rejections - 35 USC § 103***

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(f) or (g) prior art under 35 U.S.C. 103(a).

Claims 1- 5 and 12 are rejected under 35 U.S.C. 103 (c) as being anticipated by Machida et al., (US. 6,476,913 B1), in view of MacDonald, Jr. et al., (US 4,131, 472).

As per claim 1, Machida discloses a method, comprising the steps of:

(a) searching (fig 36, searching the defect on photomask by the review SEM for 1021) a defect on a photomask (fig 32, 155 wafer on which circuit pattern is formed which corresponds to photomask or reticle which is used for pattern formation in the field of semiconductor wafer by a lithography process, column 1, lines 27- 37, column 39, lines 40- 42) with a mask marking inspection system (note, fig 37, 1024 correspondence to mask marking inspection which is indicative of marking the position of defects on photomask by searching and reviewing the defect by the review SEM

1021, column 39, lines 40- 53, column 40, lines 21-34), the mask marking inspection system including a photomask inspection apparatus, and a mark installer (note, fig 36, external apparatus 1024a corresponds to mark installer, column 40, lines 21- 34) linked with the photomask inspection apparatus (fig 36, 1021 and 1024 are linked together, column 39, line 65 through column 40, line 34); and

(b) disposing a defect finder mark on the photomask with the mark installer (fig 36, 1021 SEM search for defects like foreign matter and pattern defect, or by marking the position of the pattern defect by the external device 1024a, column 39, line 65 through column 40, line 34).

Machida is silent about eliminating the defect finder mark from the photomask. mask repair device.

MacDonald, Jr. et al., discloses a photographic process manufactures integrated circuits. A wafer of semiconductor material of a selected type
Is coated with a photoresistive material and then a mask is placed over the wafer and subjected to a light source. In the production of integrated circuits, this process may be repeated a number of times using several different photomasks in a desired sequence in order to produce the finished semiconductor chip. Thus, the chip consists of a plurality of layers and patterns produced in this fashion from separate photomasks laid one at a time in precise alignment with one another. The system comprises of:

(c) repairing the defect (column 2, lines 13- 34, column 3, lines 19-24), and

(d) eliminating the defect finder mark (column 4, lines 6- 42, 57, column 5, lines 17- 34).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Machida to include repairing the defect and eliminating the defect finder mark. It would have been obvious to one of ordinary skill in the art at the time of the invention to have modified Machida by the teaching of MacDonald, in order to determining the defective chips after the manufacturing process to ascertain the predominance of defective chips having common identification numbers, than referring to the master photomask or its appropriate submaster plate for detection of the source of the defect to determine if it exists in the photo mask, followed by correction or elimination of the defect and reproduction of an improved photomask may be repeated many times, continually improving the master photomask and its related tooling such that the potential output yield obtainable by the manufacturer is greatly enhanced. By continually repeating the inspection, repair and retooling process, the photo mask manufacturer aims at achieving an essentially perfect photomask or one that is as nearly as defect-free as possible (as suggested by MacDonald at column 5, lines 17- 34).

As to claim 12, see the rejection of claim 1 above.

As to claim 2, Machida discloses the method wherein the step of searching for a defect on a photomask includes the step of locating a defect on the photomask (fig 32, 155 wafer on which circuit pattern is formed which corresponds to photomask or reticle which is used for pattern formation in the field of semiconductor wafer by a lithography process, column 1, lines 27- 37, column 39, lines 40- 42).

As to claim 3, Machida discloses the method wherein the step of searching for a

defect includes the step of searching for the defect about a dense pattern array of the photomask (note, searching the defects on circuit pattern which corresponds to dense pattern, column 17, lines 16- 24, column 23, lines 24- 35).

As to claim 4, Machida discloses the method wherein the step of searching for a defect includes the step of searching for an elusive defect (note, the defect information under the wafer map corresponds to elusive defect, column 35, lines 26- 39).

As to claim 5, Machida discloses the method wherein the step of disposing a defect finder mark on the photomask includes the step of establishing a location of the defect finder mark that is adjacent to the defect (column 2, lines 20 –29, column 6, lines 16-22).

5. Claims 6, 7, 13-19, are rejected under 35 U.S.C. 103(a) as being unpatentable over Machida et al., (US. 6,476,913 B1), in view of MacDonald, Jr. et al., (US 4,131, 472), as applied to claims 1- 5 and 12 above and further in view of Higashikawa (US. 6,765,673 B1).

Regarding claim 6, Machida discloses method and apparatus for inspecting a photomask, a reticle, a liquid crystal, and a fine circuit pattern of a semiconductor device, wherein the step of disposing a defect finder mark on the photomask includes the step of establishing a size for the defect finder mark so that the defect finder mark is detected (column 36, lines 26- 29, column 39, lines 40- 53, column 40, lines 20- 34). Machida also discloses manufacturing process of a semiconductor device, such as wafer deposition, surface oxidation, a film deposition, a photosensitive resist coating, a

development, etching, a resist removal and cleaning step. Machida is silent about a mask repair device.

Higashikawa discloses a method of forming a fine pattern of LSI by exposing an original plate such as a photomask to light. For example, in the case of a mask blank having a light shielding film formed on a transparent substrate, a black type defect is buried in the light shielding film pattern, and a white type defect is exposed to a pattern opening in which the light shielding pattern is not present so as to make these defects invisible when a mask is prepared. Also, if the defect is not positioned in a contour portion of the pattern, the defect can be corrected easily by, a laser repairing apparatus (column 3, lines 1- 11, column 7, lines 4 - 13, column 8, lines 1- 14).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Machida to include a mask repair device. It would have been obvious to one of ordinary skill in the art at the time of the invention to have modified Machida by the teaching of Higashikawa in order to perform a defect inspection and repair to eliminate the defect in a manner to satisfy the defect supervising standard and also to improve manufacturing yield and an effective utilization of the substrate such as mask blank (as suggested by Higashikawa at column 1, lines 25- 27, 63- 67).

As to claims 7 and 19, Machida discloses the method further comprising the step of searching for the defect finder mark on the photomask (column 39, lines 40- 53, column 40, lines 20- 34). Machida also discloses manufacturing process of a

semiconductor device, such as wafer deposition, surface oxidation, a film deposition, a photosensitive resist coating, a development, etching, a resist removal and cleaning step. Machida is silent about a mask repair device.

Higashikawa discloses a method of forming a fine pattern of LSI by exposing an original plate such as a photomask to light. For example, in the case of a mask blank having a light shielding film formed on a transparent substrate, a black type defect is buried in the light shielding film pattern, and a white type defect is exposed to a pattern opening in which the light shielding pattern is not present so as to make these defects invisible when a mask is prepared. Also, if the defect is not positioned in a contour portion of the pattern, the defect can be corrected easily by a laser repair apparatus (column 3, lines 1- 11, column 7, lines 4 - 13, column 8, lines 1- 14).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Machida to include a mask repair device. It would have been obvious to one of ordinary skill in the art at the time of the invention to have modified Machida by the teaching of Higashikawa in order to perform a defect inspection and repair to eliminate the defect in a manner to satisfy the defect supervising standard and also to improve manufacturing yield and an effective utilization of the substrate such as mask blank (as suggested by Higashikawa at column 1, lines 25- 27, 63- 67).

As to claim 13, Higashikawa discloses the back-end method further comprising the step of cleaning the photomask (column 5, lines 13-22, column 7, lines 62- 67,

column 8, lines 4-14).

As to claim 14, Higashikawa discloses the back-end method comprising the step of applying pellicle to the photomask (column 8, lines 7-14).

As to claim 15, Machida discloses the method wherein the step of searching for a defect includes the step of searching for the defect about a dense pattern array of the photomask (note, searching the defects on circuit pattern which corresponds to dense pattern, column 17, lines 16- 24, column 23, lines 24- 35).

As to claim16, Machida discloses the method wherein the step of searching for a defect includes the step of searching for an elusive defect (note, the defect information under the wafer map corresponds to elusive defect, column 35, lines 26- 39).

As to claim and 17, Machida discloses the method wherein the step of disposing a defect finder mark on the photomask includes the step of establishing a location of the defect finder mark that is adjacent to the defect (column 2, lines 20 –29, column 6, lines 16-22).

As to claim 18, see the rejection of claim 6 above.

6. Claims 10 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Machida et al., (US. 6,476,913 B1), in view of MacDonald, Jr. et al., (US 4,131, 472) in view of Higashikawa (US. 6,765,673 B1), as applied to claims 1-9, 12-20 above and further in view of Grenon et al., (US. 6,190,836 B1).

Regarding claim 10, Machida discloses method and apparatus for inspecting a photomask, a reticle, a liquid crystal, and a fine circuit pattern of a semiconductor device, wherein the step of eliminating the defect includes depositing a filling agent on

the defect finder mark. Machida also discloses manufacturing process of a semiconductor device, such as wafer deposition, surface oxidation, a film deposition, a photosensitive resist coating, a development, etching, a resist removal and cleaning step. Machida is silent about deposition a filling agent on the defect finder mark.

Grenon discloses a method of repairing defects in photomasks and the use of a coating on a photomask during steps to repair cleans and opaque defects on photomask by the use of short duration laser pulses to repair opaque defects on photomask. The system comprises of:

wherein the step of eliminating the defect includes depositing a filling agent on the defect finder mark (note, filling agent corresponds to carbon, column 4, lines 55- 67, column 5, lines 57- 62, column 10, lines 55- 65).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Machida to include deposition a filling agent on the defect finder mark. It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Machida by the teaching of Grenon in order to provide a more reliable method of correcting opaque and clear defects on photomasks (as suggested by Grenon at column 3, lines 40- 44).

As to claim 11, Grenon discloses the method further including the step of forming a photoresist image on a wafer substrate with the photomask (column 5, lines 25- 38, 57- 65).

***Contact Information***

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sheela C Chawan whose telephone number is. 571-272-7446. The examiner can normally be reached on Monday - Friday 7.30 - 4.00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bhavesh Mehta can be reached on 571-272-7453. The fax phone number for the organization where this application or proceeding is assigned is 571-272-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Sheela Chawan
Patent Examiner
Group Art Unit 2625
June 22, 2005